Q-TECH CORPORATION

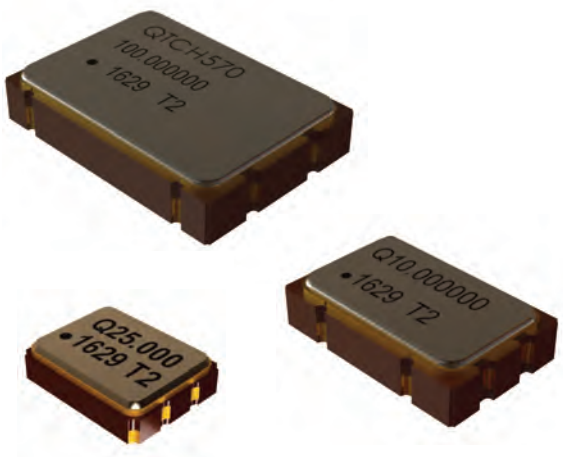
QTCH HIGH TEMPERATURE MINIATURE SMD OSCILLATORS

5 x 7mm, 3.2 x 5mm, 2.5 x 3.2mm, SMD UP TO 200°C
*1.8Vdc, 2.5Vdc and 3.3Vdc - 1MHz to 48MHz**

Description

The QTCH series are miniature surface-mount (SMD) crystal oscillators supporting a frequency between 1MHz and 48MHz* fundamental mode operating in a wide supply voltage range from 1.8Vdc to 3.3Vdc, very low power consumption (<3mA) with a temperature range from -55ºC to +200ºC. Package offerings in three low profile cermaic packages, 2.5x3.2mm, 3.2x5.0mm and 5.0x7.0mm, which are hermetically sealed with gold plated contacts or hot solder dipped.

*** Consult factory for frequencies >48MHz**



Features

- ECCN: EAR99
- Capable to work at multiple supply voltages
- Wide operating temperature -55ºC to +200ºC available
- Very low power consumption
- CMOS logic 1.8Vdc, 2.5Vdc, 3.3Vdc
- Tri-State Output Standard
- Fundamental amode AT cut crystal
- High shock and vibration resistant
- Full or partial military screening tests available
- Tape and reel packaging
- Lead Free, RoHS Compliant

Applications

- Drilling, data logging tools
- Oil service industry
- High temperature applications

Ordering Information

Sample part number

QTCH350LD12M-20.000MHz							
QTCH	350	M	D	92	M	-	20.000MHz

Package

570	=	5.0 x 7.0mm
350	=	3.2 x 5.0mm
230	=	2.5 x 3.2mm

Logic & Supply Voltage:

M	=	HCMOS +1.8Vdc to +3.3Vdc at 15pF

Tristate

D	=	Tristate

Output Frequency

Screening

Blank	=	Unscreened
M	=	Per MIL-PRF-55310, Level B

Frequency vs. Temperature Code:

87	=	±	150ppm	at	-20ºC	to +185ºC
88	=	±	200ppm	at	-20ºC	to +175ºC
89	=	±	250ppm	at	-40ºC	to +175ºC
90	=	±	200ppm	at	-40ºC	to +185ºC
91	=	±	250ppm	at	-40ºC	to +185ºC
92	=	±	250ppm	at	-55ºC	to +185ºC
93	=	±	200ppm	at	0ºC	to +200ºC
94	=	±	250ppm	at	0ºC	to +200ºC
95	=	±	250ppm	at	-20ºC	to +200ºC
96	=	±	250ppm	at	-40ºC	to +200ºC
97	=	±	250ppm	at	-55ºC	to +200ºC
98	=	±	250ppm	at	00ºC	to +185ºC

Other Options Available For An Additional Charge

- Hot Solder Dip to your specifications

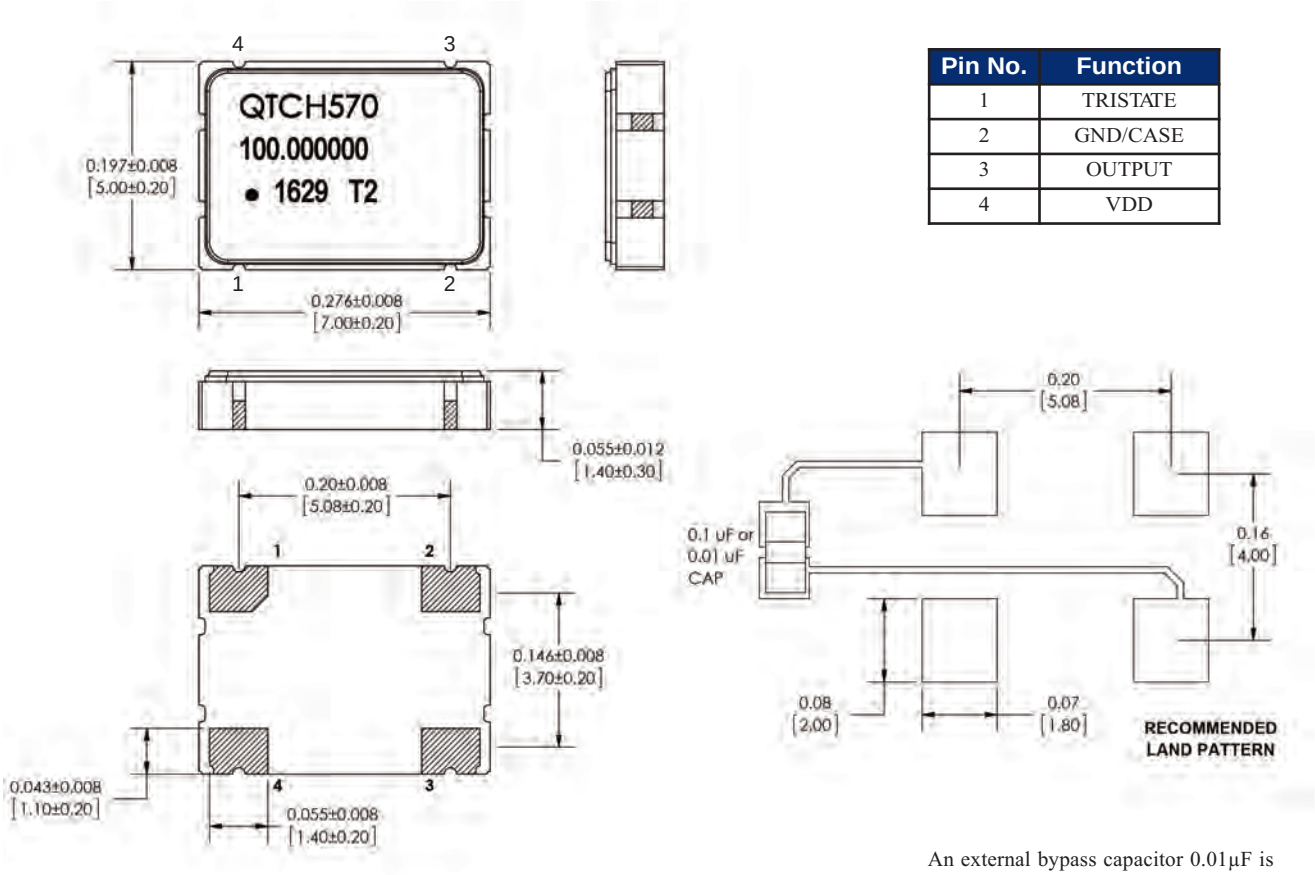
Specifications subject to change without prior notice.

Frequency stability vs. temperature codes may not be available in all frequencies.

For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com

QTCH570 Package Outline and Pin Connections

Dimensions are in inches (mm)



Pin No.	Function
1	TRISTATE
2	GND/CASE
3	OUTPUT
4	VDD

An external bypass capacitor 0.01µF is required between Vdd and GND

Marking

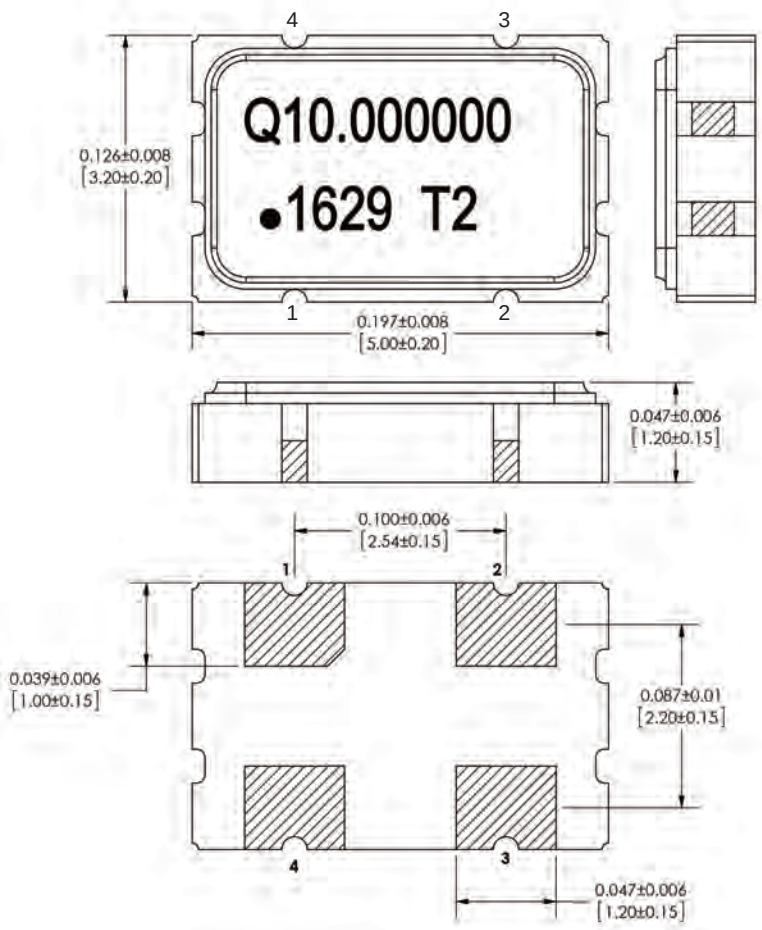
Line 1: QTCH570 (First 7 Characters of Description)
Line 2: XXX.XXXXXX (9 or 10 Characters of Frequency in MHz including decimal)
Line 3: Dot (Pin 1 Indicator) + Date code (YY/MM), Internal Traceability Code

Package Information

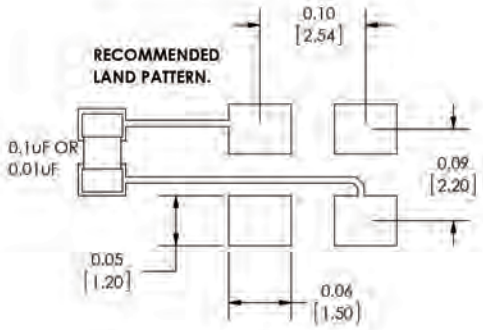
- Termination pads (4x), Electro nickel plating 1.27µm ~ 8.89µm typ., with gold 0.3µm ~ 1.0µm flash plate
- Weight: 0.15g typ., 2.0g max.

QTCH350 Package Outline and Pin Connections

Dimensions are in inches (mm)



Pin No.	Function
1	TRISTATE
2	GND/CASE
3	OUTPUT
4	VDD



An external bypass capacitor 0.01µF is required between Vdd and GND

Marking

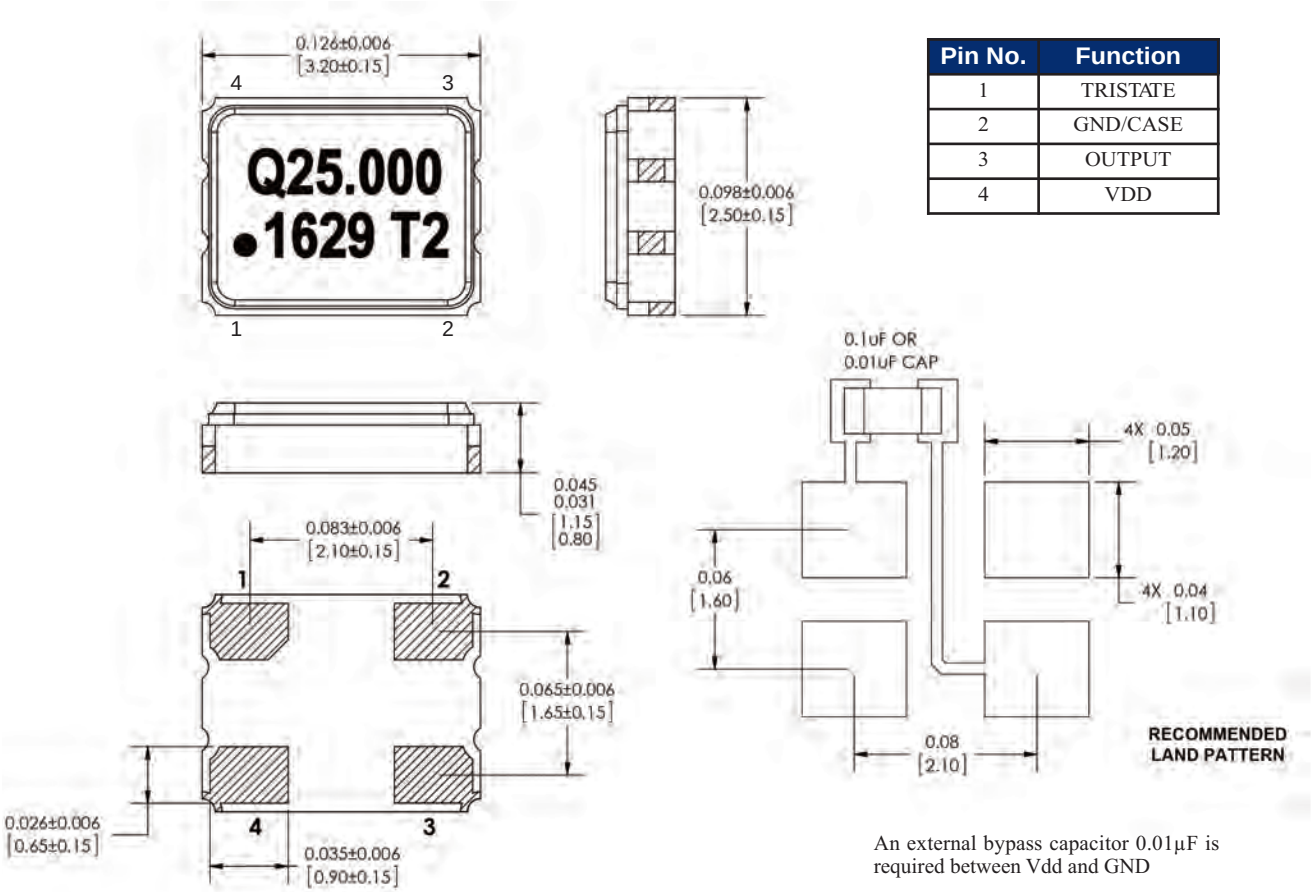
Line 1: QXXX.XXXXXX (Q for Q-Tech, no space 9 or 10 Characters of Frequency including decimal)
Line 2: Dot (Pin 1 Indicator) + Date code (YY/MM), Internal Traceability Code

Package Information

- Termination pads (4x), Electro nickel plating 1.27µm ~ 8.89µm typ., with gold 0.3µm ~ 1.0µm flash plate
- Weight: 0.15g typ., 2.0g max.

QTCH230 Package Outline and Pin Connections

Dimensions are in inches (mm)



Pin No.	Function
1	TRISTATE
2	GND/CASE
3	OUTPUT
4	VDD

An external bypass capacitor 0.01µF is required between Vdd and GND

Marking

Line 1: QXX.XXX (Q for Q-Tech, no space 7 Characters of Frequency including decimal)
Line 2: Dot (Pin 1 Indicator) + Date code (YY/MM), Internal Traceability Code

Package Information

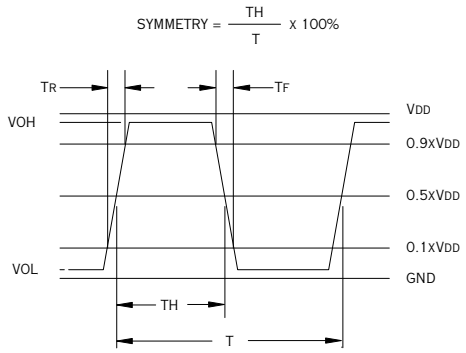
- Termination pads (4x), Electro nickel plating 1.27µm ~ 8.89µm typ., with gold 0.3µm ~ 1.0µm flash plate
- Weight: 0.15g typ., 2.0g max.

Electrical Characteristics

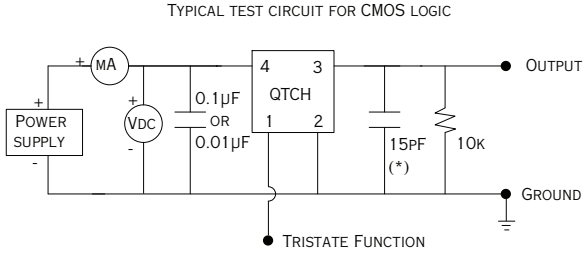
Parameters	QTCH-MD		
Output frequency range (Fo) 1/	**1.000MHz — 48.000MHz**		
Supply voltage (Vdd) 2/	1.8Vdc ± 10%	2.5Vdc ± 10%	3.3Vdc ± 10%
Maximum Applied Voltage (Vdd max.)	-0.3 to +4.0Vdc		
Frequency stability (ΔF/ΔT)	See Part Number on Page 1		
Operating temperature (Topr)	See Part Number on Page 1		
Storage temperature (Tsto)	-62ºC to + 125ºC		
Operating supply current (No Load)	2mA max.		3mA max.
Symmetry (50% of ouput waveform)	45/55%		
Rise and Fall times	6ns max.		
Output Load	15pF max.		
Start-up time (Tstup)	10ms max.		
High Output Voltage (Voh)	0.9*Vdd min.		
Low Output Voltage (Vol)	0.1*Vdd max.		
Enable VIH Pin 1	VIH ≥ 0.7*Vdd Active		
Disable VIL Pin 1	VIL ≤ 0.3*Vdd High Impedance		
Aging	±5ppm/first year		

Notes
1/ Consult factory for frequencies greater than 48MHz
2/ Part is designed to work from 1.8Vdc to 3.3Vdc. Supply voltage code is used to test the part to specific nominal voltage specified in a Purchase Order.

Output Waveform (Typical)



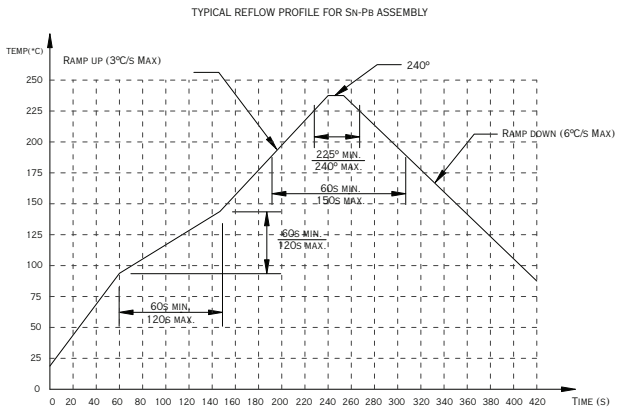
Test Circuit



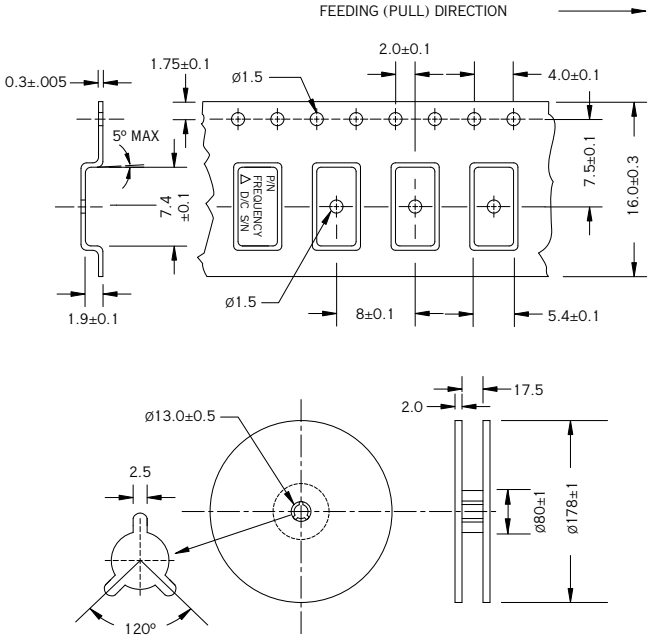
(*) CL INCLUDES PROBE AND JIG CAPACITANCE

The Tristate function on pin 1 has a built-in pull-up resistor so it can be left floating or tied to Vdd without deteriorating the electrical performance.

Reflow Profile



Embossed Tape and Reel Information



Dimensions are in mm. Tape is compliant to EIA-481-A.

Reel size (Diameter in mm)	Qty per reel (pcs)
178	1,000

Environmental and Mechanical Specifications

Environmental Test	Test Conditions
Temperature cycling	MIL-STD-883, Method 1010, Cond. B
Constant acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal: Fine and Gross Leak	MIL-STD-883, Method 1014, Cond. A and C
Vibration sinusoidal	MIL-STD-202, Method 204, Cond. D
Shock, non operating	MIL-STD-202, Method 213, Cond. I
Resistance to solder heat	MIL-STD-202, Method 210, Cond. B
Resistance to solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208
ESD Classification	MIL-STD-883, Method 3015, Class 1
Moisture Sensitivity Level	J-STD-020, MSL=1

Phase Noise and Phase Jitter Integration

Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at an offset frequency from the carrier, e.g. 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, etc. Phase noise measurement is made with an Agilent E5052A Signal Source Analyzer (SSA) with built-in outstanding low-noise DC power supply source. The DC source is floated from the ground and isolated from external noise to ensure accuracy and repeatability.

In order to determine the total noise power over a certain frequency range (bandwidth), the time domain must be analyzed in the frequency domain, and then reconstructed in the time domain into an rms value with the unwanted frequencies excluded. This may be done by converting L(f) back to Sφ(f) over the bandwidth of interest, integrating and performing some calculations.

Symbol	Definition
$\int \mathcal{L}(f)$	Integrated single side band phase noise (dBc)
$S\varphi(f)=(180/\Pi)x\sqrt{2\int \mathcal{L}(f)df}$	Spectral density of phase modulation, also known as RMS phase error (in degrees)
RMS jitter = Sφ (f)/(fosc.360°)	Jitter(in seconds) due to phase noise. Note Sφ (f) in degrees.

The value of RMS jitter over the bandwidth of interest, e.g. 10kHz to 20MHz, 10Hz to 20MHz, represents 1 standard deviation of phase jitter contributed by the noise in that defined bandwidth.

Figure below shows a typical Phase Noise/Phase jitter of a QTCH570, 3.3Vdc, 50MHz clock at offset frequencies 10Hz to 1MHz, and phase jitter integrated over the bandwidth of 12kHz to 20MHz.