

# Design Information Fact Sheet

## UT6325 RadHard Eclipse FPGA



### FEATURES

- ❑ 0.25µm, five-layer metal, ViaLink™ epitaxial CMOS process for smallest die sizes
- ❑ One-time programmable, ViaLink technology for personalization
- ❑ Typical performance characteristics -- 120 MHz 16-bit counters, 120 MHz datapaths, 60+ MHz FIFOs
- ❑ 2.5V core supply voltage, 3.3V I/O supply voltage
- ❑ Up to 320,000 system gates (non-volatile)
- ❑ I/Os
  - Interfaces with 3.3 volt
  - PCI compliant with 3.3 volt
  - Full JTAG 1149.1 compliant
  - Registered I/O cells with individually controlled enables
- ❑ Radiation-hardened design; total dose irradiation testing to MIL-STD-883 Test Method 1019
  - Total-dose: 300 krad(Si)
  - SEL Immune: >120MeV-cm<sup>2</sup>/mg
  - LET<sub>TH</sub> (0.25) MeV-cm<sup>2</sup>/mg:
    - >42 logic cell flip flops
    - >64 for embedded SRAM
  - Saturated Cross Section (cm<sup>2</sup>) per bit
    - 5.0E-7 logic cell flip flops
    - 2.0E-7 embedded SRAM
- ❑ Up to 24 dual-port RadHard SRAM modules, organized in user-configurable 2,304 bit blocks
  - 5ns access times, each port independently accessible
  - Fast and efficient for FIFO, RAM, and initialized RAM functions
- ❑ 100% routable with full logic cell utilization and 100% user fixed I/O
- ❑ Variable-grain logic cells provide high performance and 100% utilization
- ❑ Typical logic utilization = 65-80% (design dependent)

- ❑ Comprehensive design tools include high quality Verilog/VHDL synthesis and simulation
- ❑ QuickLogic IP available for microcontrollers, DRAM controllers, USART and PCI
- ❑ Packaged in a 208-pin CQFP, 288 CQFP, 484 CCGA, 484 CLGA, 208 PQFP, 280 PBGA, and 484 PBGA
- ❑ Standard Microcircuit Drawing 5962-04229
  - QML qualified

### INTRODUCTION

The RadHard Eclipse Field Programmable Gate Array Family (FPGA) offers up to 320,000 system gates including Dual-Port RadHard SRAM modules. It is fabricated on 0.25µm five-layer metal ViaLink CMOS process and contains a maximum of 1,536 logic cells and 24 dual-port RadHard SRAM modules (see Figure 1 Block Diagram). Each RAM module has 2,304 RAM bits, for a maximum total of 55,300 bits. Please reference product family comparison chart on page 2.

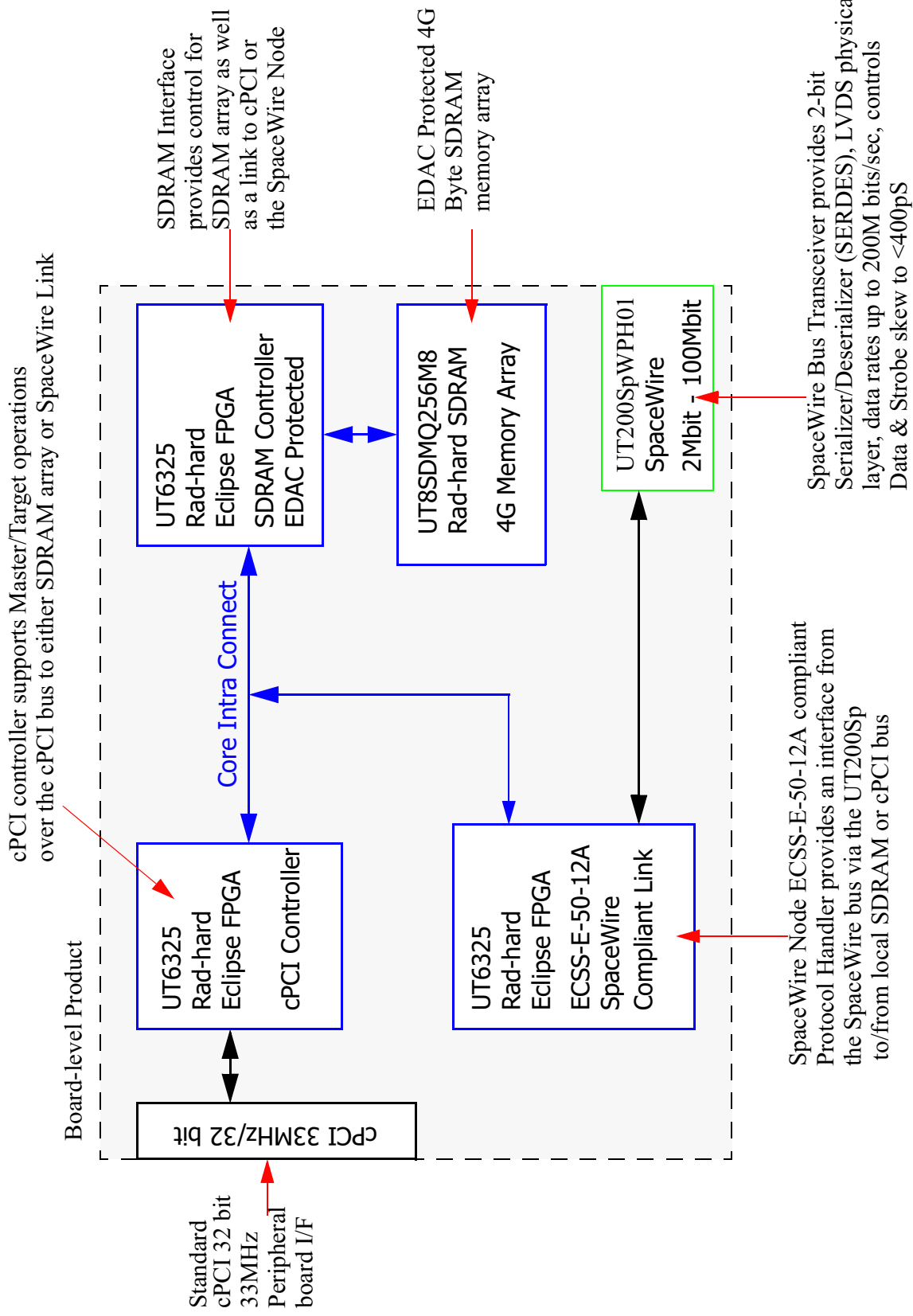
RAM modules are Dual Port (one asynchronous/synchronous read port, one write port) and can be configured into one of four modes (see Figure 2). Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules (see Figure 3). This approach allows a variety of address depths and word widths to be tailored to a specific application.

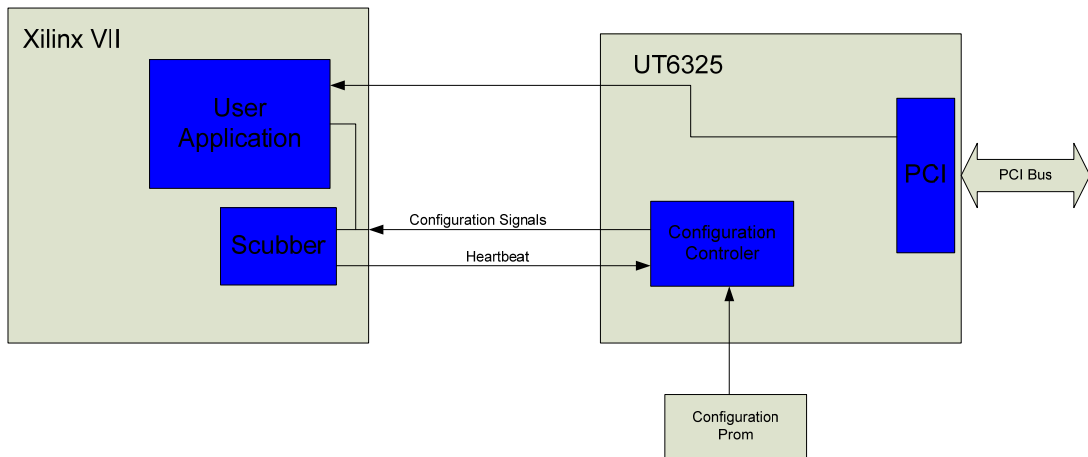
The RadHard Eclipse FPGA is available in a 208-pin Cerquad Flatpack, allowing access to 99 bidirectional signal I/O, 1 dedicated clock, 8 programmable clocks and 16 high drive inputs. Other package options include a 288 CQFP, 484 CCGA and a 484 CLGA.

Aeroflex uses QuickLogic Corporation's licensed ESP (Embedded Standard Products) technology. QuickLogic is a pioneer in the FPGA semiconductor and software tools field.

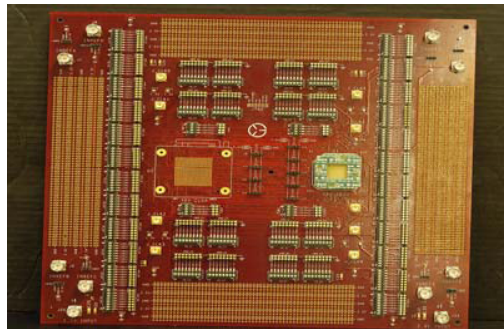
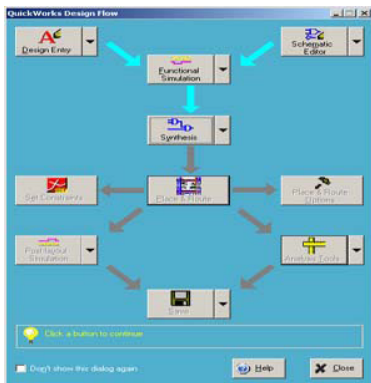


This FPGA based design enables a quick path to flight while allowing flexibility for design modifications without board revisions.



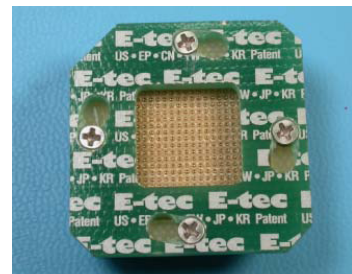
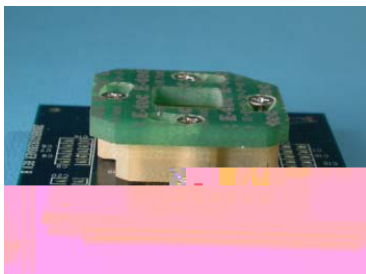
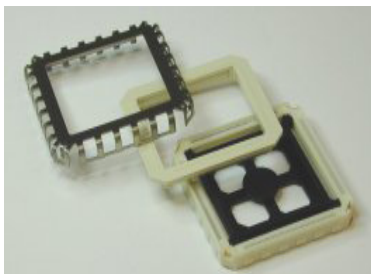


**Aeroflex RadHard Eclipse FPGA design allows the UT6325 to monitor a Xilinx scrubber, and reconfigure the scrubber circuit when any error is detected.**

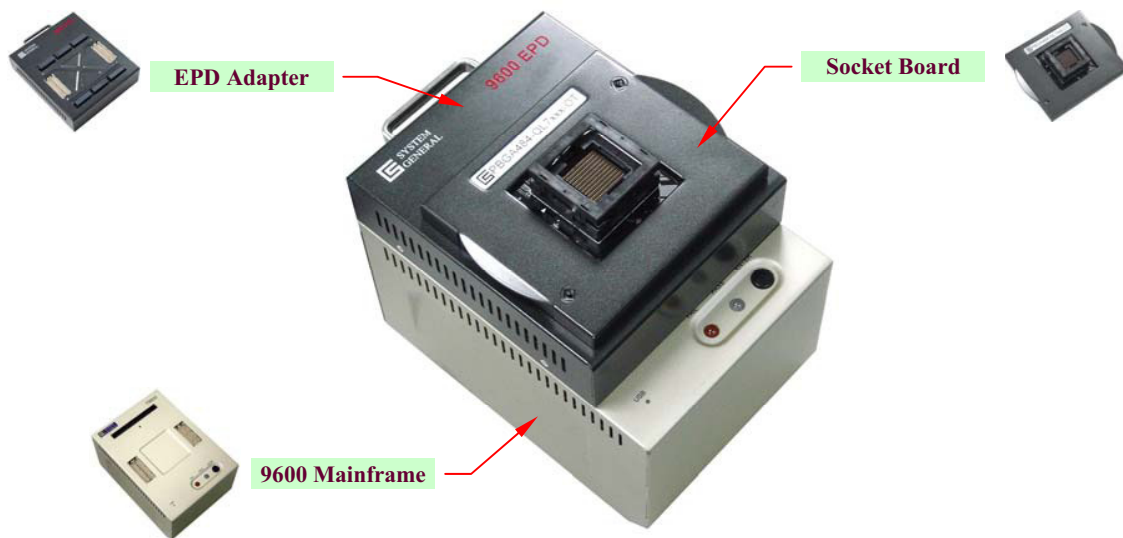


**QS-Verilog or QS-VHDL design tools include Mentor Precision Synthesis, Aldec Active-HDL Simulation and SpDE Place and Route tools .**

**UT6325 Evaluation Boards: UT8RHEEB-484P (pictured). Allows access to all I/O, high drive inputs, clocks, power planes and areas for prototype and termination.**



**Rapid Prototyping Adapters (UT8RHE-SKT208P, UT8RHE-ADP288P, UT8RHE-ADP484P). Allows users to debug in-system problems using inexpensive plastic packages and then replace the socket adapters with ceramic devices for final engineering evaluation.**



**QT-SG-T9600-A System General Programmer. Programming adapters available for both plastic (208 PQFP, 280 PBGA, 484 PBGA) and ceramic (208 CQFP, 288 CQFP, 484 CLGA, 484 CCGA) packages. Programming software optimized for Aeroflex high reliability requirements.**

**Internet Resources:**

Visit [www.aeroflex.com/RadHardFPGA](http://www.aeroflex.com/RadHardFPGA) to download:

RadHard FPGA datasheet, application notes, Rapid Prototyping, Accessories

Visit QuickLogic [www.quicklogic.com](http://www.quicklogic.com)

FPGA Development software, intellectual property, literature



**COLORADO**  
Toll Free: 800-645-8862  
Fax: 719-594-8468

**INTERNATIONAL**  
Tel: 805-778-9229  
Fax: 805-778-1980

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Fax: 603-888-4585

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Fax: 321-951-4254

**WEST COAST**  
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Fax: 949-362-2266

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